DOCKET NO. 94-C-096C1 (STMI01-94096) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	KUEI-WU HUANG ET AL
Serial No.	:	09/517,987
Filed	:	March 3, 2000
For	:	METHOD OF FORMING PLANARIZED STRUCTURES IN AN INTEGRATED CIRCUIT
Group No.	:	2812
Examiner	:	R. Booth

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellant for the application identified above. A check is enclosed for the $330.00 fee for filing a Brief on Appeal.

Applicant respectfully requests a two (2) month extension of time for filing Appellants' Brief on Appeal. The response period is presently set to expire on April 9, 2004, and if this Request for Extension of Time is granted, the new response date will be June 9, 2004. A check in the amount of $420.00 is enclosed for the two-month extension fee.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICROELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

In response to a prior appeal in this application, prosecution was reopened and a new Office Action entered. There are no other appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 77–96 are pending in the present application. Claims 77, 81–90 and 92–96 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,841,347 to *Hsu*. Claims 78–80 were rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of U.S. Patent No. 5,346,587 to *Doan et al.* Claim 91 was rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of U.S. Patent No. 5,079,180 to *Rodder et al.* Claims 77–96 were rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,422,289 to *Pierce* in view of *Doan et al.* The rejection of pending claims 77–96 is appealed.

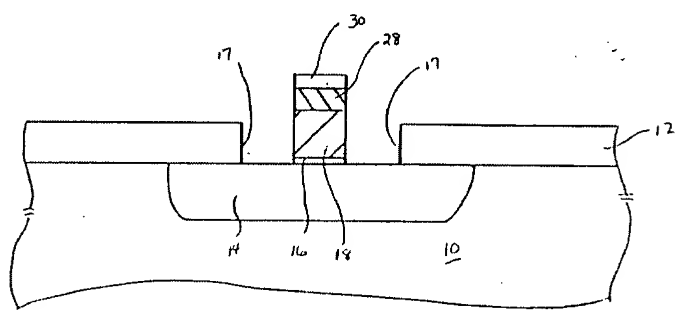
STATUS OF AMENDMENTS

No amendments to the claims were filed following the final Office Action mailed on November 6, 2003 in this matter.

SUMMARY OF THE INVENTION

The present invention relates to formation of transistor structures in integrated circuits. In the present invention, an opening having substantially vertical sidewalls is etched through a field oxide 12 over a doped well 14 within a substrate 10, and a gate electrode comprising a gate oxide 16, a an electrode comprising a polysilicon layer 18 and a silicide layer 28, and a capping layer 30 is formed within the opening:

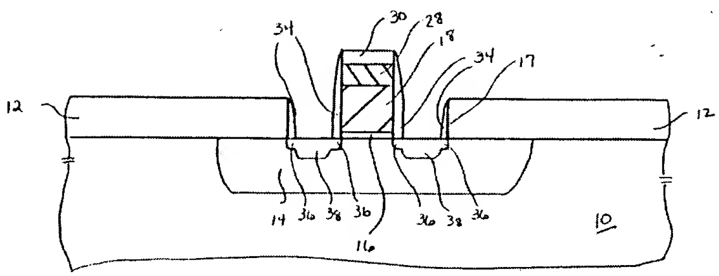
FIG. 3



Specification, Figure 3; page 9, line 14 through page 13, line 14. The polysilicon layer 18 within the gate electrode has a height above the surface of the substrate 10 that is greater than the height of the field oxide 12. Specification, page 13, lines 14–19.

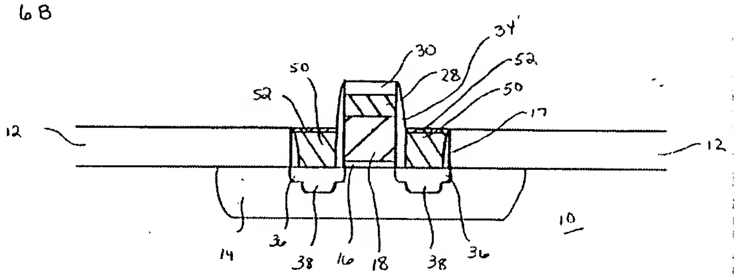
Source and drain regions are then formed adjacent the gate electrode by implanting a lightly doped region within the substrate adjacent the gate electrode, forming sidewalls 34 on the vertical surfaces of the gate electrode and the field oxide 12, and implanting a heavily doped region over lapping the light doped region, forming heavily doped source/drain regions 38 and lightly doped source drain regions 36:

FIG. 4



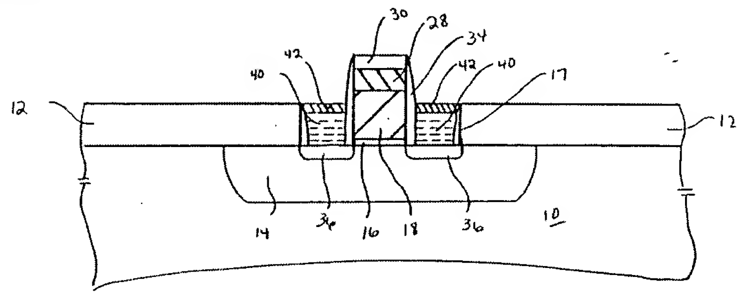
Specification, Figure 4, page 14, lines 1–12. An epitaxial layer 50 is then grown over the exposed surfaces of the substrate 10 to fill the regions over the implanted source/drain regions 36, 38 and between the sidewall spacers 34 and form raised source/drain regions 50:

FIG. 6B



Specification, Figure 6B, page 16, lines 18–20. The epitaxially grown raised source/drain regions 50 are doped to serve as heavily doped source/drain regions. In one embodiment, only lightly doped source/drain regions 36 are implanted into the substrate 10, with the heavily doped source/drain regions 40 being formed entirely above the substrate, in the epitaxially-grown raised source drain regions:

FIG. 5B



Specification, Figure 5B, page 15, lines 17–19.

ISSUES ON APPEAL

Claims 77–96 are pending in the present application. Claims 77, 81–90 and 92–96 were rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*. Claims 78–80 were rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Doan et al.* Claim 91 was rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Rodder et al.* Claims 77–96 were rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.* The issues on appeal are:

1. whether claims 77, 81–90 and 92–96 were properly rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*;
2. whether claims 78–80 were properly rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Doan et al*;
3. whether claim 91 was properly rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Rodder et al*; and

4. whether claims 77–96 were properly rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.*

GROUPING OF CLAIMS

Claims 77–96 are pending in the present application. Claims 77, 81–90 and 92–96 were rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*. Claims 78–80 were rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Doan et al.* Claim 91 was rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Rodder et al.* Claims 77–96 were rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.* For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 77–96 (all pending rejected claims);

Group B – claims 87 and 90; and

Group C – claims 93–95.

Groups A–C stand or fall independently. Patentability of the claims within each group is argued separately below.

ARGUMENT

Group A

Claims 77, 81–90 and 92–96 of Group A were rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*. Claims 78–80 of Group A were rejected under 35 U.S.C. § 103(a) as obvious over *Hsu* in view of *Doan et al.* Claim 91 of Group A was rejected under 35 U.S.C. § 103(a) as

obvious over *Hsu* in view of *Rodder et al.* Claims 77–96 of Group A were rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.* These claims are properly grouped together and considered separately from the claims of Groups B–C since they contain common limitations distinguishing the claims over the cited references, and since a decision with respect to the claims of Group A may obviate the need for consideration of Groups B–C.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-70 (8^{th} ed. rev. 1 February 2003).

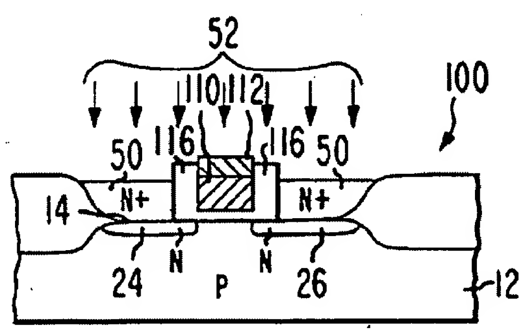
In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-123 (8th ed. rev. 1 February 2003). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant 's disclosure. MPEP § 2142 at p. 2100-124.

Independent claims 77, 93 and 96 of Group A each expressly recite that the source/drain portions within the substrate and the source/drain portions on the substrate adjacent the gate electrode together function as a source or drain for the respective device. Independent claim 77 recites that the source and drain regions each include a first portion in the substrate and a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode. Similarly, independent claim 93 recites that doped regions within the substrate and doped semiconductor material on the substrate form a source and drain for a transistor, while independent claim 96 recites that doped source and drain regions extend into the substrate and within semiconductor material on the substrate. Such a feature is not depicted or described by the cited references.

Hsu teaches a heavily doped epitaxial layer 50 formed over shallow source drain regions 24 and 26 for lowering the sheet resistance of a subsequently-formed silicide contact:

Fig. 9



Hsu, Figure 9. The layer 50 is heavily doped:

> A pair of epitaxial layers 50 of single crystalline silicon is selectively grown from the surface 14 of bare silicon directly over the source and drain regions 24 and

> 26 in the usual manner, see FIG. 4. The layers 50 should be grown to a thickness no greater than the thickness of the gate electrode 20 so that the layers 50 do not extend over the gate 20 and short the source and drain regions 24 and 26 together. The layer 50 is then subjected to a relatively high energy arsenic implantation indicated as 52 in FIG. 4, to highly dope the layer 50 down to a depth approximately equal to its thickness or slightly less.

Hsu, column 2, lines 52–63. However, *Hsu* is silent as to the heavily doped expitaxial regions 50 functioning, together with shallow source drain regions 24 and 26, as source or drain regions for the respective transistor. *Hsu* does not refer to the heavily doped epitaxial regions as source or drain regions or portions thereof. Instead, *Hsu* describes the doping of the epitaxial regions as preferably being merely sufficient to reach upwardly diffusing dopants from shallow source and drain regions 24 and 26:

> During the formation of the epitaxial layer 50, some of the impurities of the source and drain regions 24 and 26 will diffuse upwardly into the epitaxial layer 50 a short distance. Therefore, the ion implant need only reach a depth well into this upwardly diffused region. Care should be taken so that the ion implantation does not extend to a depth greater than the depth of the source and drain regions 24 and 26.

Hsu, column 2, line 63 through column 3, line 2. *Hsu* then teaches that a refractory metal silicide is formed to lower the contact resistance for a subsequently-formed metal contact:

> A layer 54 of refractory metal silicide is then formed on the highly doped epitaxial layer by depositing a layer of refractory metal, such as titanium or tungsten, and then heating the device 10 sufficiently until the refractory metal combines with the silicon at the surface 14 and thereby forming metal silicide. This layer 54 forms the desired low resistance contact to the very shallow source and drain regions 24 and 26.

Hsu, column 3, lines 2–10. Thus, *Hsu* indicates that the heavily doped epitaxial regions 50 are merely conductive connections to the shallow source and drain regions 24 and 26.

Similarly, *Pierce* discloses, in Figure 5, a structure in which the source and drain regions 34 and 36 are completely within the substrate, with conductive contacts or plugs 38 and 40 over the source and drain regions 34 and 36 are provided for electrically contacting the source and drain regions:

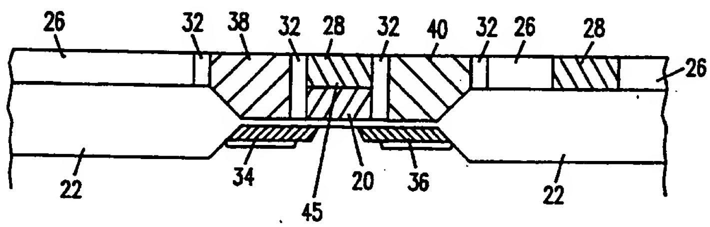


FIG. 5

Pierce teaches that conductive plugs 38, 40 may be formed from (1) deposited polysilicon planarized by chemical mechanical polishing (CMP), (2) polysilicon or single crystal silicon grown by selective chemical vapor deposition (CVD) and doped in situ, or (3) deposited metal(s) planarized by CMP. *Pierce et al*, column 11, lines 12–59. *Pierce* does not teach or suggest that the conductive plugs 38, 40 are source/drain regions, the portion of a metal oxide semiconductor field effect transistor (MOSFET) in which charge carrier (electron or hole) generation or recombination occur. *Pierce* does not teach or suggest doping the conductive plugs to function as source/drain regions, or in any manner suggest that the conductive plugs are source/drain regions or portions thereof.

The final Office Action asserts that the conductive plugs are indistinguishable from the recited source/drain regions. However, *Pierce* teaches that the conductive plugs 38 and 40 are each

a <u>conductor</u> (even if formed of doped semiconductor material), NOT a semiconductor suitable for functioning as source/drain regions. *Pierce* contains no teaching or suggest that plugs 38 and 40 function as anything other than a simple conductor, and only hindsight, with the benefit of Applicants' disclosure, allows recognition that the option of growing single crystal silicon plugs 38, 40 may, if properly doped, allow those regions to serve as a part of the source and drain for the transistor.

In the present invention, the source/drain regions are "wrapped" around the gate by formation of the raised source/drain portions, so that shallow source/drain regions implanted within the substrate may be augmented by the raised source/drain regions. The size of the source/drain regions controls, to some extent, the saturation current and the transconductance of the resulting transistor. *Pierce* contains no teaching or suggestion that the conductive plugs 38, 40 serve as "auxiliary" source/drain regions, only as simple conductors.

<u>Group B</u>

Claims 87 and 90 of Group B were rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*. Claims 87 and 90 of Group B were rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.* These claims are properly grouped together and considered separately from the claims of Groups A and C since they contain common limitations patentably distinguishing the claims over the cited references that are not found in the claims of Groups A and C.

Claims 87 and 90 of Group B each recite that the LDD regions are the first portions of the source and drain regions, the portions formed within the substrate. Such a feature is not shown in the cited references. *Hsu* teaches that heavy doping of the layer 54 formed over source and drain region need only reach the upwardly diffusing dopants from source and drain regions 24 and 26, and should not exceed the depth of the source and drain regions 24 and 26:

> During the formation of the epitaxial layer 50, some of the impurities of the source and drain regions 24 and 26 will diffuse upwardly into the epitaxial layer 50 a short distance. Therefore, the ion implant need only reach a depth well into this upwardly diffused region. Care should be taken so that the ion implantation does not extend to a depth greater than the depth of the source and drain regions 24 and 26.

Hsu, column 2, line 63 through column 3, line 2. Therefore, *Hsu* does not teach or suggest that the heavy doping of layer 54 should extend only into layer 54, leaving source and drain regions 24 and 26 lightly doped, or that the lightly doped regions should consist only of source and drain regions 24 and 26 formed within the substrate.

Group C

Claims 93–95 of Group C were rejected under 35 U.S.C. § 102(b) as anticipated by *Hsu*. Claims 93–95 of Group A were rejected under 35 U.S.C. § 103(a) as obvious over *Pierce* in view of *Doan et al.* These claims are properly grouped together and considered separately from the claims of Groups A–B since they contain common limitations patentably distinguishing the claims over the cited references that are not found in the claims of Groups A–B.

Independent claim 93 of Group C recites that "insulating material on a bottom and sides of a gate electrode forming a gate oxide between the gate electrode and a source region and between the gate electrode and a drain region." Thus, claim 93 recites that the oxide on sidewalls of the gate electrode function as a gate oxide between the gate electrode and portions of the source and drain regions beside the gate electrode--that is, the recited doped semiconductor material on the substrate within the opening adjacent to the gate structure and over each of the doped regions within the substrate that form and function, together with the doped regions within the substrate, the source and drain regions for the transistor. Such a feature is not found in the cited references.

CONCLUSION

None of the cited references, taken alone or in combination, show or suggest all features of the invention claimed in Groups A–C. Therefore, the rejections under 35 U.S.C. §§ 102 and 103 are improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 77–96 in this application.

Respectfully submitted,

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Date: 6-9-04

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CLAIMS ON APPEAL

77. An integrated circuit structure, comprising:

a substrate;

a field oxide over the substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate electrode over the surface of the substrate and within the opening, the gate electrode having insulating material on a bottom and on two sides of the gate electrode, wherein the insulating material on the bottom of the gate electrode contacts the substrate; and

source and drain regions within the substrate and adjacent the insulating material on sides of the gate electrode, each source and drain region including

a first portion in the substrate, and

a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode,

wherein the first and second portions together function as a source or drain for a device including the gate electrode.

78. The integrated circuit structure of claim 77, wherein the opening through the substrate has substantially vertical sidewalls.

79. The integrated circuit structure of claim 78, wherein each source and drain region is formed between a sidewall of the opening and the insulating material on the sides of the gate electrode.

80. The integrated circuit structure of claim 79, wherein a space between a sidewall of the opening and the insulating material on the sides of the gate electrode is filled with material forming the second portion of one of the source and drain regions.

81. The integrated circuit structure of claim 77, further comprising:

LDD regions for the source and drain regions formed within the first portion of each source and drain region.

82. The integrated circuit structure of claim 81, wherein the LDD regions are formed in the substrate beneath the insulating material on the sides of the gate electrode.

83. The integrated circuit structure of claim 77, wherein the gate electrode, the insulating material on the sides of the gate electrode, and the second portions of the source and drain regions fill a space between sidewall spacers on sidewalls of the opening.

84. The integrated circuit structure of claim 77, an upper surface of the gate electrode is further from a surface of the substrate than an upper surface of the field oxide.

85. The integrated circuit structure of claim 77, wherein the first and second portions of the source and drain regions are both formed of a semiconductor material doped to include lightly doped regions within at least the first portions and heavily doped regions within at least the second portions.

86. The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions each form contact regions for source/drain contacts.

87. The integrated circuit structure of claim 82, wherein the LDD regions are the first portions of the source and drain regions.

88. The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions have a dopant concentration suitable for heavily doped source/drain regions.

89. The integrated circuit structure of claim 88, wherein the dopant concentration within the second portions of the source and drain regions is formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

90. The integrated circuit structure of claim 88, wherein the LDD regions are the first portions of the source and drain regions.

91. The integrated circuit structure of claim 88, wherein the first portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

92. The integrated circuit structure of claim 77, further comprising:

a refractory metal silicide on the second portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

93. An integrated circuit structure, comprising:

a field oxide over a substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate structure on the surface of the substrate within the opening, the gate structure having insulating material on a bottom and sides of a gate electrode forming a gate oxide between the gate electrode and a source region and between the gate electrode and a drain region;

doped regions within portions of the substrate within the opening which are adjacent to and extend beneath the gate structure, wherein the doped regions within the substrate are at least lightly doped; and

doped semiconductor material on the substrate within the opening adjacent to the gate structure and over each of the doped regions within the substrate, the doped semiconductor material doped to a concentration suitable for heavily doped source and drain regions,

wherein each of the doped regions within the substrate and the overlying doped semiconductor material form, and together function as, either the source region or the drain region for a transistor including the gate structure.

94. The integrated circuit structure of claim 93, wherein the doped semiconductor material on the substrate has a dopant concentration formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

95. The integrated circuit structure of claim 93, wherein an upper surface of the doped semiconductor material is coated with a refractory metal silicide to form a contact region to the source and drain.

96. A transistor, comprising:

a gate electrode on an insulating layer over a substrate surface;

insulating sidewall layers on the gate electrode; and

doped source and drain regions within portions of the substrate adjacent to and extending beneath the insulating sidewall layers and within semiconductor material on the substrate adjacent to the insulating sidewall layers,

wherein the portions of the source and drain regions within the substrate are at least lightly doped and the portions of the source and drain regions within the semiconductor material on the substrate are doped to a concentration suitable for heavily doped source and drain regions,

wherein the portion of the source region within the substrate and the portion of the source region within the semiconductor material on the substrate together function as a source for the transistor, and

wherein the portion of the drain region within the substrate and the portion of the drain region within the semiconductor material on the substrate together function as a drain for the transistor.